LIQUID CRYSTAL DISPLAY DEVICE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a liquid crystal display device.

2. Description of the Related Art

In a liquid crystal display device, a liquid crystal layer formed of liquid crystal molecules is sandwiched between two sheets of insulation substrates preferably made of glass and, at the same time, at least a pair of electrodes for applying an electric field to the liquid crystal layer are provided to either one or both of the insulation substrates. In an IPS type liquid crystal display device, all of the above-mentioned electrodes for applying the electric field to the liquid crystal layer are formed on one substrate and pixels are turned on and off (that is, switching) by forming an electric field having components parallel to a substrate surface with respect to the liquid crystal layer.

SUMMARY OF THE INVENTION

Fig. 14 is an explanatory view of the vicinity of one pixel of liquid crystal display device adopting an IPS method, wherein Fig. 14A is a plan view and Fig. 14B is a cross sectional view take along a line A-A' in Fig. 14A. To an inner surface of one

substrate (first substrate, usually referred to as thin film transistor substrate since it constitutes a substrate on which thin film transistors are formed as explained hereinafter) SUB1 of a pair of substrates which constitute the liquid crystal display device, the following pixel structure is provided. Then, a second substrate SUB2 (not shown in the drawing) on which color filters and the like are formed is laminated to the first substrate SUB1 and a liquid crystal layer is sandwiched and sealed in a gap defined between both substrates.

On an inner surface of one pixel (also referred to as a unit pixel hereinafter), a plurality of scanning signal lines GL which extend in the first direction (referred to as X direction hereinafter) and are arranged in parallel in the second direction (referred to as Y direction hereinafter) which intersects the X direction, a plurality of date signal lines DL which extend in the Y direction and are arranged in parallel in the X direction, common signal lines (also referred to as common storage lines) CL which are disposed close to the scanning signal lines GL, extend in the X direction and are arranged in parallel in the Y direction, a plurality of thin film transistors TFT which are arranged at intersecting portions of the scanning signal lines GL and the date signal lines DL, pixel electrodes PX which are driven by the thin film transistors TFT, and common electrodes CT which are connected to the common signal line CL and are alternately arranged with respect to the pixel electrodes PX

such that the common electrode CT is arranged close to the pixel electrode PX in the X direction are formed. Then, unit pixels are formed in regions which are surrounded by the scanning signal lines GL and the data signal lines DL.

As shown in Fig. 14B, with respect to a cross section taken along a line A-A' in Fig. 14A, the common signal line CL is formed on the first substrate SUB1 and a date signal line and a source electrode SD of the thin film transistor TFT are formed on the common signal line CL by way of a gate insulation layer GI. These electrodes or wiring are covered with a laminated film which is constituted of an inorganic insulation layer PAS and an organic insulation layer OPAS and the pixel electrodes PX and the common electrodes CT are formed on the laminated film. Although an orientation film which is brought into contact with a liquid crystal layer not shown in the drawing is formed over the pixel electrodes PX and the common electrodes CT, these elements are omitted from the drawing here.

The pixel electrodes PX and the common electrodes CT are alternately arranged close to each other in a comb-teeth shape. As shown in Fig. 14B, the pixel electrodes PX are connected to the source electrode SD which constitutes an output electrode of the thin film transistor TFT via a through hole SH. As shown in Fig. 14A, the source electrode SD is superposed on the common signal line CL and a portion which forms the through hole SH projects into the inside of the unit pixel region in a step-like

manner. Here, reference symbol OR in the drawing indicates the direction of orientation control performance applied to the orientation film (so-called rubbing direction). Further, a range indicated by a bold dotted line virtually indicates a light blocking film (a black matrix) BM which is usually formed on the second substrate. Here, the indication of the light blocking film BM is used in respective drawings explained hereinafter in the same manner.

With respect to the liquid crystal display device having such a constitution, in a periphery of the unit pixel, particularly between the common signal line CL and the pixel electrode PX or the common electrode in the vicinity of the thin film transistor TFT, an undesired electric field is generated and this electric field gives rise to a drawback that liquid crystal molecules of the liquid crystal layer are switched irrelevant to image data thus generating a so-called image retention whereby image quality is degraded.

Fig. 15 is an explanatory view of an essential part of the detail structure of the vicinity of the thin film transistor TFT in Fig. 14A, wherein Fig. 15A is a plan view, Fig. 15B is a cross sectional view taken along a line B-B' in Fig. 15A, and Fig. 15C is a cross sectional view taken along a line C-C' in Fig. 15A.

Reference symbol ZN in Fig. 15 indicates a region where the image retention is liable to occur, reference symbol E

indicates an electric field which becomes a cause of the occurrence of image retention and reference symbol Ef indicates a particularly strong electric field. That is, as shown in Fig. 15B and Fig. 15C, due to the electric field E generated between the common signal line CL and the pixel electrode PX as well as due to the electric field E generated between the source electrode SD and the common electrode CT, the liquid crystal molecules of the liquid crystal layer are switched on and off in an undesirable manner. Further, the strong electric field Ef having a large component in the direction which intersects the liquid crystal molecules is generated between an edge of the source electrode SD and the common signal line CL which are disposed close to each other and hence, a large image retention is generated. As a result, inventers of the present invention have found that due to switching of the liquid crystal molecules irrelevant to a normal switching operation of the unit pixel, ireguralities are generated in a transmitting light (or a reflection light) whereby the image quality may be degraded.

Accordingly, it is an advantage of the present invention that the image retention is further suppressed compared to the above-mentioned liquid crystal display device having the structure shown as Fig. 14 whereby image display having high image quality can be obtained.

To achieve such an advantage, the present invention adopts respective electrode structures in which an electric field

between a common signal line and a pixel electrode is blocked, an electric field between a source electrode of a thin film transistor and a common electrode is blocked or an electric field between an edge of the source electrode and the common signal line is blocked.

The detail of these electrode structures will become apparent in view of respective embodiments which express various examples as technical concepts in conjunction with drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is an explanatory view of the constitution of the vicinity of a unit pixel in the first embodiment of a liquid crystal display device according to the present invention;

Fig. 2 is an explanatory view of an essential part of the detailed structure of the vicinity of a thin film transistor TFT in Fig. 1;

Fig. 3 is an explanatory view of the constitution of the vicinity of a unit pixel in the second embodiment of a liquid crystal display device according to the present invention;

Fig. 4 is an explanatory view of an essential part of the detailed structure of the vicinity of a thin film transistor TFT in Fig. 3;

Fig. 5 is an explanatory view of the constitution of the vicinity of a unit pixel in the third embodiment of a liquid crystal display device according to the present invention;

Fig. 6 is an explanatory view of an essential part of the detailed structure of the vicinity of a thin film transistor TFT in Fig. 5;

Fig. 7 is an explanatory view of the constitution of the vicinity of a unit pixel in the fourth embodiment of a liquid crystal display device according to the present invention;

Fig. 8 is an explanatory view of an essential part of the detailed structure of the vicinity of a thin film transistor TFT in Fig. 7;

Fig. 9 is an explanatory view of the constitution of the vicinity of a unit pixel in the fifth embodiment of a liquid crystal display device according to the present invention;

Fig. 10 is an explanatory view of an essential part of the detailed structure of the vicinity of a thin film transistor TFT in Fig. 9;

Fig. 11 is an explanatory view of the constitution of the vicinity of a unit pixel in the sixth embodiment of a liquid crystal display device according to the present invention;

Fig. 12 is an explanatory view of an essential part of the detailed structure of the vicinity of a thin film transistor TFT in Fig. 11;

Fig. 13 is a schematic cross sectional view for explaining a constitutional example of a unit pixel portion and a peripheral portion of the liquid crystal display device of the present invention;

Fig. 14 is an explanatory view of the vicinity of one pixel of a liquid crystal display device adopting an IPS method; and

Fig. 15 is an explanatory view of an essential part of the detailed structure of the vicinity of a thin film transistor TFT in Fig. 14.

DETAILED DESCRIPTION

Hereinafter, embodiments of the present invention are explained in detail in conjunction with drawings which show respective embodiments.

Fig. 1 is an explanatory view of the constitution of the vicinity of a unit pixel in the first embodiment of a liquid crystal display device according to the present invention, wherein Fig. 1A is a plan view and Fig. 1B is a cross sectional view taken along a line A-A' in Fig. 1A. Further, Fig. 2 is an explanatory view of an essential part of the detailed structure in the vicinity of the thin film transistor TFT in Fig. 1A, wherein Fig. 2A is a plan view, Fig. 2B is a cross sectional view taken along a line B-B' in Fig. 2A and Fig. 2C is a cross sectional view taken along a line C-C' in Fig. 2A. In Fig. 1 and Fig. 2, reference symbols which are equal to the reference symbols in the above-mentioned Fig. 14 and Fig. 15 correspond to identical functional portions and hence, their repeated explanation is omitted. Here, the same goes for respective embodiments described hereinafter.

In Fig. 1 and Fig. 2, on an inner surface of the unit pixel formed on a first substrate SUB1, a plurality of scanning signal lines GL which extend in the X direction and are arranged in parallel in the Y direction which intersects the X direction, a plurality of date signal lines DL which extend in the Y direction and are arranged in parallel in the X direction, common signal lines CL which are disposed close to the scanning signal lines GL, extend in the X direction and are arranged in parallel in the Y direction, a plurality of thin film transistors TFT which are arranged at intersecting portions of the scanning signal lines GL and the date signal lines DL, pixel electrodes PX which are driven by the thin film transistors TFT, and common electrodes CT which are connected to the common signal line CL and are alternately arranged with respect to the pixel electrodes PX such that the common electrode CT is arranged close to the pixel electrode PX in the X direction are formed. Then, the unit pixel is formed in a region surrounded by the scanning signal lines GL and the data signal lines DL.

The common electrodes CT are arranged in a superposed manner over the common signal line CL by way of an insulation layer which is constituted of an inorganic insulation layer PAS and an organic insulation layer OPAS stacked on the inorganic insulation layer PAS. The same goes for respective embodiments. However, in place of the organic insulation layer OPAS, an inorganic insulation layer may be used. Also in this case, the

same goes for respective embodiments described hereinafter. The pixel electrode PX is connected to the source electrode SD of the thin film transistor TFT via the through hole SH which penetrates the insulation layer which is formed of the above-mentioned inorganic insulation layer PAS and organic insulation layer OPAS. The common electrodes CT are formed such that the common electrodes CT extend (project) into the inside of the unit pixel so as to cover the common signal line CL whereby an electric field E between the common signal line CL and the pixel electrode PX is blocked.

The pixel electrode PX has an end portion extending toward the inside of the unit pixel from the common electrode CT, while the source electrode SD has a first projecting portion SD1 and a second projecting portion SD2 which project in a step-like manner in the direction which intersects the extending direction of the common electrodes CT. The step-like first projecting portion SD1 (source electrode side) is arranged between the common signal line CL and the pixel electrode PX and, at the same time, at a position which is sealed or blocked by the common electrode CT. Further, the step-like second projecting portion SD2 (a portion which further projects toward the unit pixel side from the first projecting portion SD1) is connected to the pixel electrode PX via the through hole SH at a position where the second projecting portion SD2 superposes on the pixel electrode PX.

Further, assuming a distance between an edge of the second projecting portion parallel to the Y direction and the pixel electrode PX neighboring in the X direction as "a", a distance between the pixel electrode PX and an end portion of the first projecting portion in the Y direction as "b", and a distance between the pixel electrode PX and the common electrode CT neighboring in the Y direction as "c", the relationship a>c and b>c is established. Further, the relationship a>c and b>c may be established. Due to such setting of relationships, the electric field generated between the common signal line and the pixel electrode is blocked or the electric field E generated between the source electrode SD of the thin film transistor TFT and the common electrode CT is blocked. Further, the electric field E generated between the edge of the source electrode SD and the common signal line CL is also blocked.

According to this embodiment, switching of liquid crystal molecules irrelevant to the normal switching operation of the unit pixel is suppressed and hence, no irregularities are generated with respect to a transmitting light (or a reflection light) of the liquid crystal layer whereby the high-quality image display can be obtained.

Fig. 3 is an explanatory view of the constitution of the vicinity of a unit pixel in the second embodiment of a liquid crystal display device according to the present invention, wherein Fig. 3A is a plan view and Fig. 3B is a cross sectional

view taken along a line A-A' in Fig. 3A. Further, Fig. 4 is an explanatory view of an essential part of the detailed structure in the vicinity of the thin film transistor TFT in Fig. 3A, wherein Fig. 4A is a plan view, Fig. 4B is a cross sectional view taken along a line B-B' in Fig. 4A and Fig. 4C is a cross sectional view taken along a line C-C' in Fig. 4A.

In Fig. 3 and Fig. 4, on an inner surface of the unit pixel formed on a first substrate SUB1, a plurality of scanning signal lines GL which extend in the X direction and are arranged in parallel in the Y direction which intersects the X direction, a plurality of date signal lines DL which extend in the Y direction and are arranged in parallel in the X direction, common signal lines CL which are disposed close to the scanning signal lines GL, extend in the X direction and are arranged in parallel in the Y direction, a plurality of thin film transistors TFT which are arranged at intersecting portions of the scanning signal lines GL and the date signal lines DL, pixel electrodes PX which are driven by the thin film transistors TFT, and common electrodes CT which are connected to the common signal line CL and are arranged with respect to the pixel electrodes PX such that the common electrode CT is arranged close to the pixel electrode PX in the X direction are formed. Then, the unit pixel is formed in a region surrounded by the scanning signal lines GL and the data signal lines DL.

The pixel electrode PX is arranged in a superposed manner

over the common signal line CL by way of an insulation layer (an inorganic insulation layer PAS and an organic insulation layer OPAS) and is connected to a source electrode SD of the thin film transistor TFT via a through hole SH which penetrates the above-mentioned insulation layer. Further, a portion of the pixel electrode PX overhangs over the common signal line CL beyond the unit pixel and an overhanging distal end forms an extending portion PXJ which is retracted from a side of the common signal line CL at a side opposite to the pixel electrode. The common electrodes CT are formed such that the common electrodes CT extend in the inside of the unit pixel covering the common signal line CL except for a portion along the extending portion PXJ of the pixel electrode PX. Due to such a constitution, an electric field E between the common signal line CL and the pixel electrode PX can be blocked.

Further, the extending portion PXJ of the pixel electrode PX has a width larger than a width of the pixel electrode PX in the X direction and the source electrode SD has a projecting portion SD3 which projects in a step-like manner in the direction which intersects the extending direction of the common signal line CL. The step-like projecting portion SD3 is arranged between the common signal line CL and the common electrode CT and is arranged at a position which is blocked by the common electrode CT. The step-like projecting portion SD3 is arranged above the common signal line CL and at a position where the

projecting portion SD3 superposes on an extending portion PXJ of the pixel electrode PX and is connected to the pixel electrode PX via the through hole SH.

Then, assuming a distance of the step-like projecting portion SD3 of the source electrode SD from an end portion of the common signal line CL in the Y direction as "a", a distance in the X direction of the edge in the Y direction parallel to the common signal line CL contiguous with the extending portion PXJ of the pixel electrode PX as "b", and a distance in the X direction between the edge in the Y direction of the overhanging portion PXJ of the pixel electrode PX and the common electrode CT as "c", the relationship $a \geq 0$ is established. Further, the relationship $b > c \times 2.0$ is established. Further, the relationship $a \geq 0$ and $b > c \times 2.0$ is established. Due to such setting of relationships, the electric field E between the common signal line CL and the pixel electrode PX is blocked or the electric field E generated between the source electrode SD of the thin film transistor TFT and the common electrode CT is blocked. Further, the electric field E generated between the edge of the source electrode SD and the common signal line CL is also blocked.

According to this embodiment, switching of liquid crystal molecules irrelevant to the normal switching operation of the unit pixel is suppressed and hence, no irregularities are generated with respect to a transmitting light (or a reflection light) of the liquid crystal layer whereby the high-quality image

display can be obtained.

Fig. 5 is an explanatory view of the constitution of the vicinity of a unit pixel in the third embodiment of a liquid crystal display device according to the present invention, wherein Fig. 5A is a plan view and Fig. 5B is a cross sectional view taken along a line A-A' in Fig. 5A. Further, Fig. 6 is an explanatory view of an essential part of the detailed structure in the vicinity of the thin film transistor TFT in Fig. 5A.

In Fig. 5 and Fig. 6, on an inner surface of the unit pixel formed on a first substrate SUB1, a plurality of scanning signal lines GL which extend in the X direction and are arranged in parallel in the Y direction, a plurality of date signal lines DL which extend in the Y direction and are arranged in parallel in the X direction, common signal lines CL which are disposed close to the scanning signal lines GL, extend in the X direction and are arranged in parallel in the Y direction, a plurality of thin film transistors TFT which are arranged at intersecting portions of the scanning signal lines GL and the date signal lines DL, pixel electrodes PX which are driven by the thin film transistors TFT, and common electrodes CT which are connected to the common signal line CL and are arranged with respect to the pixel electrodes PX such that the common electrode CT is arranged close to the pixel electrode PX in the X direction are formed. Then, the unit pixel is formed in a region surrounded by the scanning signal lines GL and the data signal lines DL.

The pixel electrode PX is arranged in a superposed manner over the common signal line CL by way of an insulation layer (an inorganic insulation layer PAS and an organic insulation layer OPAS) and is connected to a source electrode SD of the thin film transistor TFT via a through hole SH which penetrates the insulation layer(the inorganic insulation layer PAS and the organic insulation layer OPAS). Further, a portion of the pixel electrode PX includes an enlarged portion PXE which strides over the common signal line CL from the inside of the unit pixel. The common electrodes CT are formed such that the common electrodes CT extend in the inside of the unit pixel covering the common signal line CL except for a portion along the enlarged portion PXE of the pixel electrode PX. Due to such a constitution, an electric field between the common signal line CL and the pixel electrode PX can be blocked.

The enlarged portion PXE of the pixel electrode PX has an approximately rectangular shape having two sides along the X direction of the unit pixel and another two sides along the Y direction, wherein the unit-pixel-side side out of two sides along the X direction extends into and is positioned in the inside of the unit pixel beyond the common signal line CL, while the side opposite to the unit pixel out of two sides along the X direction is positioned inside an edge of the common signal line CL at a side opposite to the unit pixel and outside an edge of the source electrode SD at a side opposite to the unit pixel.

Then, assuming a distance "a" between the pixel electrode PX which extends in the Y direction from the enlarged portion PXE to the inside of the unit pixel and the common electrode CT which is arranged close to the pixel electrode PX in the X direction as "a", a distance between two sides of the enlarged portion PXE along the X direction and the common electrodes CT which are arranged close to the enlarged portion PXE as "b" and a distance between the unit pixel-PX-side side out of two sides along the X direction and the common signal line CL as "c", a relationship $a>b$ is established or a relationship $b\times0.5<c$ is established. Further, a relationship $a>b$ and $b\times0.5<c$ is established. In this manner, by enlarging the pixel electrode PX, a region which can block the common signal line CL can be enlarged whereby the electric field E between the common signal line CL and the pixel electrode PX can be blocked or the electric field between the source electrode SD of the thin film transistor TFT and the common electrode CT can be blocked. Further, the electric field between the edge of the source electrode SD and the common signal line CL can be also blocked.

Fig. 7 is an explanatory view of the constitution of the vicinity of a unit pixel in the fourth embodiment of a liquid crystal display device according to the present invention, wherein Fig. 7A is a plan view and Fig. 7B is a cross sectional view taken along a line A-A' in Fig. 7A. Further, Fig. 8 is an explanatory view of an essential part of the detailed structure

in the vicinity of the thin film transistor TFT in Fig. 7A.

This embodiment is characterized in that portions of the common signal line CL have a width thereof narrowed at both sides of the projecting portion SD4 of the source electrode SD in the embodiment 3, wherein a unit-pixel-side edge of the common signal line CL is retracted such that a distance between the unit-pixel-side edge of the common signal line CL and the unit-pixel-side side in the X direction of the enlarged portion PXE of the pixel electrode PX is increased. That is, in the region of a portion of the source electrode SD2 which is covered with the enlarged portion PXE of the pixel electrode PX, in the X direction of the projecting portion SD4 which projects toward the unit pixel side and also projects in a step-like manner at the unit pixel side than the common signal line CL, a unit-pixel-side edge of the common signal line CL which is arranged at the data signal line DL side is retracted at a side opposite to the unit pixel and the relationship distance a > distance b is established.

According to this embodiment, in addition to the advantageous effects of the third embodiment, switching of liquid crystal molecules irrelevant to the normal switching operation of the unit pixel can be further suppressed and hence, no irregularities are generated with respect to a transmitting light (or a reflection light) of the liquid crystal layer whereby the high-quality image display can be obtained.

Fig. 9 is an explanatory view of the constitution of the vicinity of a unit pixel in the fifth embodiment of a liquid crystal display device according to the present invention, wherein Fig. 9A is a plan view and Fig. 9B is a cross sectional view taken along a line A-A' in Fig. 9A. Further, Fig. 10 is an explanatory view of an essential part of the detailed structure in the vicinity of the thin film transistor TFT in Fig. 9A, wherein Fig. 10A is a plan view and Fig. 10B is a cross-sectional view taken along a line B-B' in Fig. 10A.

In Fig. 9 and Fig. 10, on an inner surface of the unit pixel formed on a first substrate SUB1, a plurality of scanning signal lines GL which extend in the X direction and are arranged in parallel in the Y direction, a plurality of date signal lines DL which extend in the Y direction and are arranged in parallel in the X direction, common signal lines CL which are disposed close to the scanning signal lines GL, extend in the X direction and are arranged in parallel in the Y direction, a plurality of thin film transistors TFT which are arranged at intersecting portions of the scanning signal lines GL and the date signal lines DL, pixel electrodes PX which are driven by the thin film transistors TFT, and common electrodes CT which are connected to the common signal line CL and are arranged with respect to the pixel electrodes PX such that the common electrode CT is arranged close to the pixel electrode PX in the X direction are formed. Then, the unit pixel is formed in a region surrounded

by the scanning signal lines GL and the data signal lines DL.

The pixel electrode PX is arranged in a superposed manner over the common signal line CL by way of an insulation layer (an inorganic insulation layer PAS and an organic insulation layer OPAS) and is connected to a source electrode SD of the thin film transistor TFT via a through hole SH which penetrates the insulation layer (the inorganic insulation layer PAS and the organic insulation layer OPAS). Further, a portion of the pixel electrode PX includes an enlarged portion PXE which strides over the common signal line CL from the inside of the unit pixel.

The common electrodes CT are formed such that the common electrodes CT extend in the inside of the unit pixel covering the common signal line CL except for a portion along the enlarged portion PXE of the pixel electrode PX and hence, an electric field between the common signal line CL and the pixel electrode PX can be blocked. The enlarged portion PXE of the pixel electrode PX has two sides along the X direction of the unit pixel and two sides along the Y direction. The unit-pixel-side side out of two sides along the X direction is positioned inside a unit-pixel-side edge (side) of the common signal line CL, while the side out of two sides opposite to the unit pixel PX is positioned outside the edge of the common signal line CL opposite to the unit pixel and outside the edge of the enlarged portion PXE of the pixel electrode PX opposite to the unit pixel.

A side of the source electrode SD of the thin film transistor

TFT opposite to the unit pixel extends in the X direction close to the thin film transistor TFT to form one side of an extending portion SDE, while another side of the source electrode SD at the unit pixel side extends in the X direction parallel to one side of the extending portion SDE at the side opposite to the unit pixel from side of another two sides in the Y direction close to the thin film transistor TFT. Then, assuming a distance between another side of the extending portion SDE and the edge of the common signal line CL opposite to the unit pixel PX as "a" and a distance between the side opposite to the unit pixel PX out of another two sides of the source electrode SD and the neighboring common electrode in the X direction as "b", these distances are set as $a \geq 0$ and $b \geq 0$.

Accordingly, as shown in Fig. 10B, a portion where a fringe electric field Ef which constitutes a strong electric field formed between the source electrode SD and the common signal line CL can be completely blocked by the pixel electrode PX and hence, switching of liquid crystal molecules irrelevant to the normal switching operation of the unit pixel can be further suppressed whereby no irregularities are generated with respect to a transmitting light (or a reflection light) of the liquid crystal layer whereby the high-quality image display can be obtained.

Fig. 11 is an explanatory view of the constitution of the vicinity of a unit pixel in the sixth embodiment of a liquid

crystal display device according to the present invention, wherein Fig. 11A is a plan view and Fig. 11B is a cross sectional view taken along a line A-A' in Fig. 11A. Further, Fig. 12 is an explanatory view of an essential part of the detailed structure in the vicinity of the thin film transistor TFT in Fig. 11A.

In Fig. 11 and Fig. 12, on an inner surface of the unit pixel formed on a first substrate SUB1, a plurality of scanning signal lines GL which extend in the X direction and are arranged in parallel in the Y direction, a plurality of date signal lines DL which extend in the Y direction and are arranged in parallel in the X direction, common signal lines CL which are disposed close to the scanning signal lines GL, extend in the X direction and are arranged in parallel in the Y direction, a plurality of thin film transistors TFT which are arranged at intersecting portions of the scanning signal lines GL and the date signal lines DL, pixel electrodes PX which are driven by the thin film transistors TFT, and common electrodes CT which are connected to the common signal line CL and are arranged with respect to the pixel electrodes PX such that the common electrode CT is arranged close to the pixel electrode PX in the X direction are formed. Then, the unit pixel is formed in a region surrounded by the scanning signal lines GL and the data signal lines DL.

The pixel electrode PX is arranged in a superposed manner over the common signal line CL by way of an insulation layer (an inorganic insulation layer PAS and an organic insulation

layer OPAS) and is connected to a source electrode SD of the thin film transistor TFT via a through hole SH which penetrates the insulation layer (the inorganic insulation layer PAS and the organic insulation layer OPAS).

Further, a portion of the pixel electrode PX includes an approximately rectangular enlarged portion PXE which strides over the common signal line CL from the inside of the unit pixel, while the source electrode SD includes a projecting portion SD4 which projects toward the unit pixel side at a portion which is covered with the enlarged portion PXE of the pixel electrode PX and projects toward the unit pixel side in a step-like manner beyond the common signal line.

The common electrode CT is formed such that the common electrode CT extends (overhangs) in the inside of the unit pixel while covering the common signal line CL except for a portion of the common signal line CL along the enlarged portion PXE of the pixel electrode PX so as to block an electric field between the common signal line CL and the pixel electrode PX. At the same time, the common electrode CT includes common electrode enlarged portions CTE which are enlarged to cover the common signal lines CL corresponding to the enlarged portion PXE of the pixel electrode PX at portions of the thin film transistor TFT side while having sides which extend at an angle θ in the X direction with respect to the Y direction and sides which extend in the Y direction. Here, an angle at which the pixel electrode

PX in the unit pixel rises is also set to θ.

The enlarged portions PXE of the pixel electrode PX include two sides along the X direction of the unit pixel and two another sides which extend in the Y direction of the unit pixel, wherein the unit-pixel-side side out of two sides along the X direction is positioned in the more inside of the unit pixel than the common signal line CL and another side of the two sides opposite to the unit pixel is positioned in the more inside than an edge the common signal line CL opposite to the unit pixel.

Here, by setting the angle θ to $90° \leq \theta < 180°$, the pixel electrode PX and the common electrode CT are enlarged. Further, the relationship between a distance "a" between the side of the common electrode enlarged portion CTE which extends in the X direction and the step-like edge extending along the first direction, a distance "b" between the unit-pixel-side edge of the common signal line CL and the edge along the X direction of the projecting portion SD4 of the source electrode SD which projects in a step-like manner, and a distance "c" between the pixel electrode PX and the edge in the Y direction of the common electrode enlarged portion CTE is set to $a>b$ and is preferably set to $(a-b)>c$. Due to such a constitution, an electric field from the common signal line CL can be surely blocked and hence, the image retention areas are reduced whereby the effective numerical aperture can be increased.

Here, in the above-mentioned respective embodiments, by

setting the distance between the pixel electrode PX and the source electrode SD in Fig. 1 smaller than the distance between the pixel electrode PX and the common electrode CT which are arranged to close each other, for example, a DC component which remains between the electrodes can be reduced and hence, the image retention can be suppressed and, at the same time, the effective numerical aperture is enhanced. Here, as shown in Fig. 14, by forming a black matrix BM such that the black matrix BM covers longitudinal end portions of the pixel electrodes PX and the common electrodes CT in the inside of the unit pixel, the degradation of image quality attributed to the image retention can be further suppressed.

Further, in the above-mentioned respective embodiments, by further arranging the common signal lines CL along both sides of the scanning signal line GL, it is possible to have an effect for blocking leaking of the electric field from the scanning signal line GL. Here, the end portions of common electrodes CT are formed such that the end portions are retracted from the common electrodes CT in the inside of the unit pixel.

Fig. 13 is a schematic cross-sectional view for explaining a constitutional example of the unit pixel portion and the peripheral portion of the liquid crystal display device of the present invention. In the drawing, SUB1 indicates the first substrate which is explained in conjunction with respective embodiments. A first orientation film is applied to an uppermost

layer which is brought into contact with the liquid crystal layer LC and rubbing treatment is applied to the first orientation film. Then, a first polarizer POL1 is formed on an outer surface. Here, reference symbols which are equal to the references symbols used in the foregoing explanation correspond to identical functional portions, wherein PSV indicates a protective film and the constitution of the first substrate SUB1 is simplified. Further, SUB2 indicates the second substrate which constitutes the counter substrate, wherein the second substrate SUB2 includes color filters CF which are defined by the black matrix BM and an overcoat layer OC which is formed above the color filters CF. Further, a second orientation film ORI2 which is brought into contact with the liquid crystal layer LC is applied to the overcoat layer OC and rubbing treatment is applied to the second orientation film ORI2. A second polarizer POL2 is mounted on an outer surface (a viewing side) of the second substrate SUB2. A sealing material seals between peripheral portions of the first substrate SUB1 and the second substrate SUB2. The electric field EP which performs switching of the unit pixel (turning on/off of the unit pixel) is formed between the pixel electrode PX and the common electrode CT in the direction parallel to the respective substrate surfaces.

As has been explained heretofore, according to the present invention, the generation of the undesired electric field between the common signal lines and the pixel electrodes and the common

electrodes in the periphery of the unit pixel, particularly in the vicinity of the thin film transistor can be suppressed and hence, the occurrence of image retention can be reduced whereby it is possible to provide the liquid crystal display device which is capable of displaying the high quality images.